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Patent

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Atsushi MIYANISHI et al.	)	Group Art Unit: 2815
	)	
Application No.: 09/114,203	)	Examiner: Bradley W. Baumeister
	)	
Filed: July 13, 1998	)	Confirmation No: 8932
	)	
For: SEMICONDUCTOR DEVICE	)	Appeal No. unassigned

BRIEF FOR APPELLANT

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: March 10, 2003

Sir:

This appeal is from the decision of the Primary Examiner dated October 16, 2002 (Paper No. 32) in which claims 13-24 were rejected in a Final Office Action and claims 2-4 and 6-11 were withdrawn from consideration. Claims 13-24 are reproduced Appendix A. In addition, Figures 24-28 are provided in Appendix B.

A check covering the [ ] $160.00 (2402) [X] $320.00 (1402) Government fee and two extra copies of this brief are being filed herewith.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 02-4800. This paper is submitted in triplicate.

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I. Real Party in Interest

The present application is assigned to Mitsubishi Denki Kabushiki Kaisha, who is the real party in interest.

II. Related Appeals and Interferences

There are no currently known pending related appeals and interferences in the subject application.

III. Status of Claims

Claims 13-24 are rejected, and claims 2-4 and 6-11 are withdrawn from consideration. Claims 1, 4, 5 and 12 have been previously cancelled without prejudice.

IV. Status of Amendments

A final Office Action was issued on October 16, 2002. This Brief is filed in response to that Office Action.

V. Summary of the Invention

The present invention relates to a semiconductor device, and more particularly, it relates to the shape of a margin part of a gate electrode forming a MOS transistor which is provided on an active area having a concave part. (page 1, lines 5-7)

In the semiconductor device according to the present invention, the margin part of the first gate electrode has a sufficient length, whereby the end portion of the first gate electrode completely reaches the upper portion of the insulating film even if an unnecessary active area exists in the concave part of the active area after various fabrication steps, whereby the first gate electrode is prevented from partial reduction of its gate length. Therefore, occurrence of current leakage between the source/drain regions formed on the exterior of both side surfaces of the first gate electrode is prevented, whereby a normally operating MOS transistor can be obtained. (page 8, lines 14-22)

Fig. 24 shows a part of an active area 10 in the layout design phase of a modification of the semiconductor device according to the embodiment 4 of the present invention and gate electrodes 20 and 30H arranged on this active area 10. Referring to Fig. 24, the active area 10 has a concave part in a portion other than the corner portion in a shape along a plan view. An insulating film 7 encloses the active area 10. in this case, the concave part may alternatively be referred to as a dent part. (page 32, lines 11-17)

The gate electrode 30H is arranged on a depressed region DR having an edge portion which is located on a low position due to the concave part. Ordinary regions (regions other than the depressed region) OR1 and OR2 (first and second ordinary regions) having edge portions projecting beyond the depressed region DR are provided on both sides of the depressed region DR. The gate electrode 20 is arranged on the ordinary region OR1. A gate end cap of the gate electrode 20 has a length x. (page 32, lines 18-24)

An end portion of the ordinary region OR2 is located on a position depressed from that of an end portion of the ordinary region OR1, to result in difference between the depression lengths of the ordinary regions OR1 and OR2. A gate end cap of the gate electrode 30H is formed to project beyond an edge portion of the ordinary region OR2 by a length substantially equal to the length x of the gate end cap of the gate electrode 20 arranged on the ordinary region OR1. (page 32, line 25 through page 33, line 5)

Fig. 25 shows a part of an active area 10A of a semiconductor device actually fabricated on the basis of such design values and gate electrodes 20 and 30H arranged on this active area 10A. Referring to Fig. 25, the active area 10A has a concave part which is not rectangularly shaped. A gate end cap of the gate electrode 30H is formed to project beyond an edge portion of an ordinary region OR2 by a length substantially equal to the length x of a gate end cap of the gate electrode 20 arranged on an ordinary region OR1 in the active area 10A having such a shape, whereby an end portion of the gate electrode 30H completely reaches an upper portion of an insulating film 7 even if an unnecessary active area exists in the concave part of the active area 10A, thereby preventing the gate electrode 30H from partial reduction of its gate length. Thus, occurrence of current leakage between source/drain regions SDA and SDB can be prevented, whereby the function of the MOS

transistor can be maintained. If no problem arises in the fabrication process but no unnecessary region exists in the concave part, a semiconductor device similar to that shown in Fig. 24 is obtained, as a matter of course. (page 33, lines 7-22)

While the gate end cap of the gate electrode 30H is formed to project beyond the edge portion of the ordinary region OR2 by the length substantially equal to the length x of the gate end cap of the gate electrode 20 arranged on the ordinary region OR1 as hereinabove described in the aforementioned semiconductor device according to the embodiment 4, the length of such a gate end cap may alternatively set in the following manner: (page 33, line 24 through page 34, line 4)

Fig. 26 shows a part of an active area 10 in the layout design phase of a modification 1 of the semiconductor device according to the embodiment 4 of the present invention and gate electrodes 20 and 301 arranged on this active area 10. Referring to Fig. 26, the gate electrode 301 is arranged on a depressed region DR, and the gate electrode 20 is arranged on an ordinary region OR1. (page 34, lines 5-9)

A gate end cap of the gate electrode 20 has a length x, while a gate end cap of the gate electrode 301 is so formed as to project beyond a position where a virtual line VL connecting two convex corner portions K1 and K2 of the concave part of the active area 10 intersects with the gate electrode 301, i.e., a position where the virtual line VL intersects with a longer side closer to the ordinary region OR1 in two longer sides of the gate end cap by a length substantially equal to the length x. (page 35, lines 10-16)

The position where the virtual line VL intersects with the gate electrode 301 may be defined as that where the virtual line VL intersects with the center line of the gate electrode 301 or with a longer side closer to the ordinary region OR2 in two longer sides of the gate electrode 301. (page 35, lines 17-20)

Fig. 27 shows a part of an active area 10A of a semiconductor device actually fabricated on the basis of such design values and a gate electrode 301 arranged on this active area 10A. Referring to Fig. 27, the active area 10A has a concave part which is not rectangularly shaped. *A* gate end cap of the gate electrode 301 is formed to project beyond an intersection between a virtual line VL and the gate electrode 301 by a length

substantially equal to a length x, whereby an end portion of the gate electrode 301 completely reaches an upper portion of an insulating film 7 even if an unnecessary active area exists in the concave part of the active area 10A, thereby preventing the gate electrode 301 from partial reduction of its gate length. Thus, occurrence of current leakage between source/drain regions SDA and SDB can be prevented, whereby the function of the MOS transistor can be maintained. If no problem arises in the fabrication process and no unnecessary region exists in the concave part, a semiconductor device similar to that shown in Fig. 26 is obtained, as a matter of course. (page 34, line 21 through page 35, line 9)

While the ordinary regions OR1 and OR2 are different in depression length from each other in the aforementioned semiconductor device according to the embodiment 4 of the present invention, the length of a gate end cap may be set in the following manner if depression lengths on right and left sides of a concave part are identical to each other. (page 35, lines 11-15)

Fig. 28 shows a part of an active area 100 in the layout design phase of a modification 2 of the semiconductor device according to the embodiment 4 of the present invention and gate electrodes 20 and 30J arranged on this active area 100. The active area 100 shown in Fig. 28 is provided with depressed portions having the same length on right and left sides of a concave part. The gate electrode 30J is arranged on a depressed region OR having an edge portion which is located on a low position due to the concave part, and the gate electrode 20 is arranged on an ordinary region OR1. (page 35, lines 16-23)

A gate end cap of the gate electrode 30J is so formed as to project beyond an edge portion of the depressed region OR by a length substantially equal to the length x of a gate end cap of the gate electrode 20 arranged on the ordinary region OR1. Even if the concave part is filled up with an unnecessary active area to disappear, source/drain regions SDA and SDB provided on both sides of the gate electrode 30J are electrically isolated from each other and prevented from shorting due to the aforementioned structure, whereby the function of the MOS transistor can be maintained. (page 35, line 24 through page 36, line 6)

VI. The Issues

The issues presented for review are:

1) whether claims 13, 17-19, 23 and 24 were properly rejected under 35 U.S.C. §103 as obvious over *Shou et al.* (U.S. Patent No. 5,811,859) in view of *Bergemont* (WO 94/29898); and

2) whether claims 14-16 and 20-23 were properly rejected under 35 U.S.C. §103 as being unpatentable over *Shou et al.* and *Bergemont* and further in view of *Jassowski et al.* (U.S. Patent No. 5,668,389).

VII. Grouping of Claims

Applicants respectfully submit that claims 17-18, 23 and 24 do not stand or fall together with claims 13 and 19 as a group since these claims are separately patentable as discussed below. Furthermore, Applicants respectfully submit that claim 14-16 and 20-23 do not stand or fall together as a group since these claims are separately patentable as discussed below.

VIII. Applicants arguments against the rejection of claims 13, 17-19, 23 and 24 under 35 U.S.C. §103

A. Errors in the Rejection

Applicants respectfully submit that the rejection of claims 13, 17-19, 23 and 24 is erroneous because the difference between the claimed subject matter and the cited prior art is such that the invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. Applicants respectfully submit that the Examiner is only selecting bits and pieces from those references without considering the remaining teaching of those references which would lead away from the claimed invention. Furthermore, Applicants respectfully submit that the Examiner is misinterpreting *Shou et al.* and impermissibly modifying *Bergemont* in light of Applicants teachings.

B. Limitations not Described in the Prior Art

The limitation not described in the prior art is that the length of the second gate electrode, from the third edge to the first end thereof, is greater than the length of the first gate electrode from the fourth edge to the first end thereof.

C. Explanation of Why the Limitation Renders the Claim Subject Matter Unobvious Over the Prior Art

Shou et al. appears to disclose in FIG. 3, a LSI pattern of inverted amplifier INV consisting of 3 stages MOS invertors, I1, I2 and I3. For the invertors I1 and I2, there are shaped a common P-type semiconductor layer PL1 and a common N-type semiconductor layer NL1. P-type semiconductor layer PL2 and N-type semiconductor layer NL2 are shaped for I3. Drain voltage Vdd and source voltage Vss are connected to PL1 and NL1 through contacts C1 and C2. A contact is a metal part passing through in semiconductor layer in the direction of thickness, for electrical connection. The drain-voltage Vdd and source voltage Vss are connected to PL2 and NL2 through contacts C7 and C8. The semiconductor layers PL1 and NL1 are provided with contacts C3 and C4 for an output from the first stage, respectively, and are provided with contacts C5 and C6 for an output from the second stage, respectively. The semiconductor layers PL2 and NL2 are provided with contacts C9 and C10 for an output from the third stage, respectively, from which an output is introduced through a poly-silicon portion PS toward the next stage. A strangulation portion S1 is provided between the contacts C1 and C5 in the semiconductor layer PL1, and a strangulation portion S3 is provided between the contacts C2 and C6 in the semiconductor layer NL1. A strangulation portion S2 is provided between contacts C7 and C9 in the semiconductor layers PL2, and a strangulation portion S4 is provided between contacts C8 and C10 in the semiconductor layer NL2. These strangulation means S1 and S3 limit an electric current of the output of inverter I2, and it simultaneously decreases parasitic capacity of a transistor included in the inverter I2 by decreasing electric currency. (col. 2, line 44 through col. 3, line 8)

Thus, *Shou et al.* merely discloses active region PL1 having a strangulation region S1 and including a first gate electrode G disposed between contacts C3, C1, and a second gate electrode G disposed between contacts C1, C5. Nothing in *Shou et al.* shows, teaches or suggests that both the first and second gate electrodes extend beyond the edge of the region PL1. In other words, nothing in *Shou et al.* shows, teaches or suggests a first gate electrode has a first end which extends beyond the fourth edge and a second gate electrode has a first end which extends beyond a third edge as claimed in claim 13 and 19. Rather, only one of the gate electrodes in *Shou et al.*, in the strangulation region, extends beyond the strangulation.

Additionally, as clearly shown in Figure 3 of *Shou et al.*, since only one of the gate electrodes G, G extends beyond the edge of the PL1 region, nothing in *Shou et al.* shows, teaches or suggests a) first and second gate electrodes, which extend beyond edges, each having a length from the edge or b) that the length extending beyond the edge of the second gate electrode is greater than the length extending beyond the edge of the first gate electrode as claimed in claims 13 and 19. Rather, *Shou et al.* clearly discloses that only the gate electrode in the strangulation extends beyond the edge of the PL1 region.

Applicants respectfully traverse the Examiner's statement that it is inherent or at least obvious to provide an end cap on the ordinary region. Applicants respectfully submit that it is impossible to provide an end cap or margin part without the recognition of the problems that arise when there is no end cap or margin part. However, there is no recognition in *Shou et al.* as is obviously shown in Figure 3 thereof. That is, in the ordinary region PL1 of *Shou et al.*, the edge of the gate electrode G is shown so that it matches the edge portion of the active region PL1. Applicants respectfully submit that if *Shou et al.* recognized the problem of not providing an end cap, *Shou et al.* would have described the edge of the gate electrode G as projecting beyond the edge portion of the active region PL1. However, no description is made within the body of the patent and neither is anything shown in Figure 3 of *Shou et al.* Rather, *Shou et al.* is directed to providing a strangulation portion in the active region constructing an inverter and providing a gate electrode on the strangulation portion. Thus according to *Shou et al.* the

gate width is shortened and consequently the output current is controlled. Thus nowhere in *Shou et al.* is there any recognition of the margin part of the gate electrode. As proof, Applicants again respectfully point out that there is no description with regard to the gate electrode having a margin part in the description portion corresponding to Figure 3 in the specification of *Shou et al.* Rather, *Shou et al.* merely discloses that the position of the strangulation portion is explained with relation to the contact portion.

Additionally, Applicants respectfully point out to the Examiner that the length of the gate G and strangulation portion S1 in *Shou et al.* extends only to the edge of the PL region. Thus nothing in *Shou et al.* shows, teaches or suggests that the second length is greater than the lengths of the first and second edges as claimed in claims 17 and 23 or that the first end of the first gate electrode and the first end of the second gate electrode are in a line as claimed in claims 18 and 24.

Bergemont appears to disclose, according to conventional single poly integrated circuit fabrication techniques, all of the polysilicon lines in the circuit are defined simultaneously utilizing a single mask step. That is, a layer of polysilicon (poly1) is first formed over the entire device structure. A poly 1 photoresist mask is then formed and pattern to define the underlying polysilicon. A single etch step is then performed to define individual poly1 lines. As shown in Fig. 1A, the fabrication process specification defines the desired offset distances "a" and "b" for the "end caps" of the individual polysilicon lines in both the x-direction and the y-direction, respectively. However, rather than the substantially rectangular (90^0) geometry shown in Fig. 1A, in reality, the final geometry of both the field oxide island 10 and the end cap of the polysilicon line 12 is more "rounded", as shown in Fig. 1B. The field oxide rounding effect is inherent to the type of field isolation and photolithographic process used. The poly end cap rounding effect is inherent to the photolithography of small polysilicon lines. As shown in Fig. 1B, these physical rounding effects result in a reduced width of the polysilicon lines 10 at the poly1/field oxide interface. Thus, when the poly1 line is used as a self-aligned mask for the implementation of dopant to create the source and drain regions of MOS transistors in the circuit, the channel length of the MOS device is reduced, leading to undesirable current

leakage from one side of the poly1 to the other. Any misalignment of the poly1 mask further exacerbates this leakage problem, as shown in Fig. 1C. To avoid this problem, prior art techniques rely on larger design rules. That is, design rules for the length of the poly end cap, the distance between the poly end cap and the parallel edge of the field oxide, and the width of the poly1 line all may be increased. These steps insure that the channel length of each of the MOS devices in the circuit is greater than an acceptable minimum required to prevent leakage.

Thus, *Bergemont* merely discloses desired offset distances for end caps in the x and y directions. Nothing in *Bergemont* shows, teaches or suggests a) first and second gate electrodes or b) the length of a second gate electrode beyond a third edge is greater than the length of the first gate electrode beyond the fourth edge as claimed in claims 13 and 19. Rather, *Bergemont* merely discloses offset distances for individual end caps in the x and y directions.

Applicants note that page 1, lines 30-33 of *Bergemont* disclose increasing the length of the poly end cap, the distance between the poly end cap and the parallel edge of the oxide field and the width. However, Applicants respectfully submit that nowhere in *Bergemont* does it show, teach or suggest that the lengths of different end caps would be different from one another.

Finally, since *Bergemont* only discloses offset distances from individual end caps, nothing in *Bergemont* shows, teaches or suggests the second length is greater than the lengths of the first and second edges as claimed in claims 17 and 23 or that the first end of the first and second gate electrodes are in a line as claimed in claims 18 and 24.

D. Why The References Taken as a Whole Do Not Suggest The Claimed Invention And Why The Features Disclosed in One Reference May Not Be Properly Combined With The Features Disclosed in The Other Reference.

As discussed above *Shou et al.* clearly shows in Figure 3 only the electrode G associated with the strangulation S1 extends beyond the edge of the PL1 region. Thus nothing in *Shou et al.* shows, teaches or suggests that the second gate electrode has a

length from a third edge which is greater than the length of the first gate electrode from a fourth edge as claimed in claims 13 and 19. Furthermore, as discussed above, *Bergemont* merely discloses desired offset distances for end caps. However, nowhere in *Bergemont* is it shown, taught or suggested that the lengths of different end caps would be different from one another.

The combination of *Shou et al.* and *Bergemont* would merely suggest to define the same offset distances for the end caps in both the X and Y direction as taught by *Bergemont* to the two gate electrodes in the PL1 region of *Shou et al.* Thus nothing in the combination of *Shou et al.* and *Bergemont* shows, teaches or suggests that the length of the second gate electrode beyond the third edge is greater than the length of the first gate electrode beyond the fourth edge as claimed in claims 13 and 19.

Additionally, Applicants respectfully submit that it is neither obvious nor inherent to provide an end cap on the gate electrode in *Shou et al* since nowhere in *Shou et al.* is there any description for a margin part for Fig. 3. Furthermore, Applicants respectfully submit that even if it is obvious or inherent to provide an end cap on the gate electrode of *Shou et al.* based upon *Bergemont*, nothing in the combination of *Shou et al* and *Bergemont* shows, teaches or suggests that the length of the second gate electrode beyond the third edge is greater than the length of the first gate electrode beyond a fourth edge as claimed in claims 13 and 19.

Furthermore, neither reference alone or in combination show, teach or suggest the features as claimed in claims 17-18 or 23-24 as discussed above.

For all of the above stated reasons, Applicants respectfully request that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's rejection of claims 13, 17-19, 23 and 24 under 35 U.S.C. §103.

IX. Applicants Arguments Against the Rejection of Claims 14-16 and 20-23 under 35 U.S.C. §103

A. Errors in the Rejection

Applicants respectfully submit that the rejection claims 14-16 and 20-23 is erroneous because the difference between the claimed subject matter and the cited prior art is such that the invention would not have been obvious to a person of ordinary skill in the art at the time the invention was made. Applicants respectfully submit that the Examiner is only selecting bits and pieces from both references without considering the remaining teachings of those references which would lead away from the claimed invention. Furthermore, Applicants respectfully submit that the Examiner is misinterpreting *Shou et al.* and *Bergemont* and impermissibly modifying *Jassowski et al.* in light of Applicants teachings.

B. Limitations Not Described in the Prior Art

The limitations not described in the prior art are:

a) the first edge is greater in length than the second edge and the second length is greater than at least the length of the second edge as claimed in claims 14 and 20,

b) the second length is a sum of the first length and the length of the second edge as claimed in claims 15 and 21,

c) the second length is the sum of the first length and a length of a third edge to an intersection of the second gate electrode and an imaginary line connecting the second end of the first edge and a second end of the second edge as claimed in claims 16 and 22, and

d) that the second length is greater than the lengths of the first and second edges as claimed in claim 23.

C. Explanation of Why the limitations render the claimed subject matter unobvious over the prior art.

As discussed above, *Shou et al.* only discloses that the gate electrode in the strangulation region extends beyond the strangulation. Nothing in *Shou et al.* shows, teaches or suggests the length of the second gate electrode beyond the third edge is greater than the length of the first gate electrode beyond the fourth edge. Furthermore, *Shou et al.* merely discloses a u-shaped strangulation. Therefore, nothing in *Shou et al.* shows, teaches or suggests a first edge is greater in length than a second edge and that the second length is greater than at least the length of the second edge as claimed in claim 14 and 20. Furthermore, since Figure 3 of *Shou et al.* merely discloses that the gate G in strangulation S1 extends to the edge of the PL1 region, nothing in *Shou et al.* shows, teaches or suggests a second length is a sum of a first length and the length of the second edge as claimed in claims 15 and 21 or that the second length is the sum of the first length and the length from the third edge to an intersection with a second gate electrode and an imaginary line connecting the second end of the first edge and the second end of the second edge as claimed in claims 16 and 22. Furthermore, since the gate G of *Shou et al.* in the strangulation S1 only extends up to the end of the PL1 region, nothing in *Shou et al.* shows, teaches or suggests that the second length is greater than the lengths of the first and second edges as claimed in claim 23.

As discussed above, *Bergemont* merely discloses desired offset distances for end caps. Nothing in *Bergemont* shows, teaches or suggests that the length of the second gate electrode beyond a third edge is greater than the length of the first gate electrode beyond the fourth edge. Furthermore, *Bergemont* merely discloses a rectangular FOX area. Nothing in *Bergemont* shows, teaches or suggests that a first edge is greater in length than a second edge and the second length is greater than at least the length of the second edge as claimed in claims 14 and 20. Furthermore, *Bergemont* only discloses desired offset distances for end caps. Nothing in *Bergemont* shows, teaches or suggests that the second length is the sum of the first length and the length of the second edge as claimed in claims 15 and 21 or that the second length is the sum of the first length and a length from a third

edge to an intersection of the second gate electrode and an imaginary line connecting the second end of the first edge and a second end of the second edge as claimed in claims 16 and 22. Finally, nothing in *Bergemont* shows, teaches or suggests that the second length is greater than the lengths of the first and second edges as claimed in claim 23. *Bergemont* only discloses desired offset distances of the end caps.

Jassowski et al. depicts in Figure 2 as labeled by the Examiner gates G0-G4 and edges E1-E5. Upon review of the Figure 2 of *Jassowski et al.* it is respectfully submitted that all the end caps labeled by the Examiner and all other unlabeled end caps with the exception of the end cap associated with G1 are all equal in length. Only the end cap for G1 is longer than any of the other end caps. However, this end cap G1 is not associated with a gate electrode extending over a third edge as defined in claims 13 and 19. Rather, the gate electrode G4 is analogous to the second gate electrode claimed in claims 13 and 19. However, the length of the gate electrode G4 from the third edge E3 labeled by the Examiner is not greater than the length of the first gate electrode from a fourth edge E4 as claimed in claims 13 and 19. Rather, as clearly shown in Figure 2, the lengths of the end caps of gate G4 and G3 are equal. Furthermore, since the lengths of the end caps of G4 and G3 in Figure 2 of *Jassowski et al.* are equal, nothing in *Jassowski et al.* shows, teaches or suggests a) the second length is greater than at length of the second edge as claimed in claims 14 and 20, b) the second length is the sum of the first length and the length of the second edge as claimed in claims 15 and 21, c) the second length is the sum of the first length and the length from the third edge to an intersection of the second gate electrode and an imaginary line connecting the second end of the first edge and the second end of the second edge as claimed in claims 16 and 22 or d) the second length is greater than the lengths of the first and second edges as claimed in claim 23.

D. Why the references taken as a whole do not suggest the claimed invention and why the features disclosed in one reference may not be properly combined with the features disclosed in the other references.

The combination of *Shou et al.*, *Bergemont* and *Jassowski et al.* would merely suggest to define the same offset distances for all end caps as taught by *Bergemont*, and make all offset distances the same for all end caps as taught by *Jassowski et al.* for the two gate electrodes in the PL 1 region of *Shou et al.* Thus nothing in the combination of the references shows, teaches or suggests a) that the length of the second gate electrode beyond the third edge is greater than the length of the first gate electrode beyond the fourth edge, b) that the second length is greater than at least the length of the second edge, c) the second length is the sum of the first length and the length of the second edge, d) the second length is the sum of the first length and the length from the third edge to an intersection of the second gate electrode and an imaginary line or e) the second length is greater than the lengths of the first and second edges as claimed in claims 14-16 and 20-23.

For all of the above stated reasons, Applicants respectfully request that the Honorable Board of Patent Appeals and Interferences reverses the Examiner's rejection of claims 14-16 and 20-23 under 35 U.S.C. §103.

X. Conclusion

For all of the above stated reasons, Applicants respectfully request the Honorable Board of Patent Appeals and Interferences reverses the Examiner's decision in this case since Applicants respectfully submit that the final rejection of claims 13-24 is in error. Therefore, Applicants respectfully submit that claims 13-24 should be allowed.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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APPENDIX A

The Appealed Claims

13. A semiconductor device comprising:

an active area with at least one MOS transistor to be formed therein; and

an insulation film for defining said active area,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends, said first gate electrode having a first end extending beyond said fourth edge over said insulation film,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, said second gate electrode having a first end extending beyond said third edge over said insulation film,

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the length of said second gate electrode being greater than the length of said first gate electrode.

14. The semiconductor device according to claim 13, wherein
said first edge is greater in length than said second edge, and
said second length is greater than at least the length of said second edge.

15. The semiconductor device according to claim 14, wherein
said second length is a sum of said first length and the length of said second edge.

16. The semiconductor device according to claim 14, wherein
said second length is a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

17. The semiconductor device according to claim 13, wherein
said second length is greater than the lengths of said first and second edges.

18. The semiconductor device according to Claim 17, wherein
said first and second gate electrodes are parallel to each other, and
said first end of said first gate electrode and said first end of said second gate electrode are in a line.

19. A method of manufacturing a semiconductor device including an active area with at least one MOS transistor to be formed therein, and an insulation film for defining said active area, based on layout design comprising the steps of:
(a) configuring said active area to have a recess in plan configuration; and
(b) configuring a first MOS transistor having a first gate electrode and a second MOS transistor having a second gate electrode on said active area,
said step (a) including the steps of
configuring said recess to be defined by first, second and third edges, said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and a first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend, and

configuring a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said step (b) including the steps of

configuring said first gate electrode to extend in a direction perpendicular to the direction in which said fourth edge extends and to have a first and end extending beyond said fourth edge over said insulation film, and

configuring said second gate electrode to extend in a direction perpendicular to the direction in which said third edge extends and to have a first end extending beyond said third edge over said insulation film,

said first gate electrode beyond said fourth edge being defined by having a first length from said fourth edge to said first end thereof, said second gate electrode beyond said third edge being defined by having a second length from said third edge to said first end thereof, the length of said second gate electrode being greater than the length of said first gate electrode.

20. The method according to claim 19, wherein

said step (a) includes configuring said first edge to be greater in length than said second edge, and

said step (b) includes configuring said second length to be greater than at least the length of said second edge.

21. The method according to claim 20, wherein

said step (b) includes configuring said second length to equal a sum of said first length and the length of said second edge.

22. The method according to claim 20, wherein

said step (b) includes configuring said second length to equal a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

23. The method according to claim 19, wherein

said step (b) includes configuring said second length to be greater than the lengths of said first and second edges.

24. The method according to claim 23, wherein

said step (b) includes

configuring said first and second gate electrodes to be parallel to each other, and

configuring said first end of said first gate electrode and said first end of said second gate electrode to be in a line.

APPENDIX B

Figures 24-28

FIG. 24

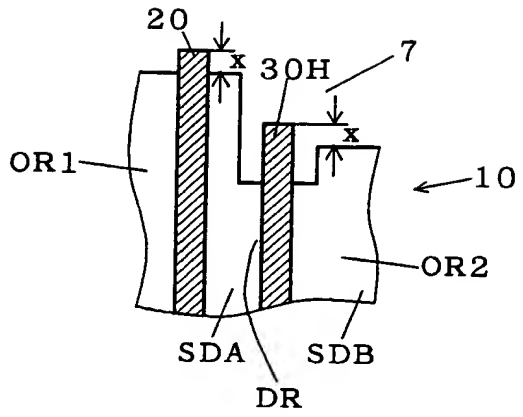

FIG. 25

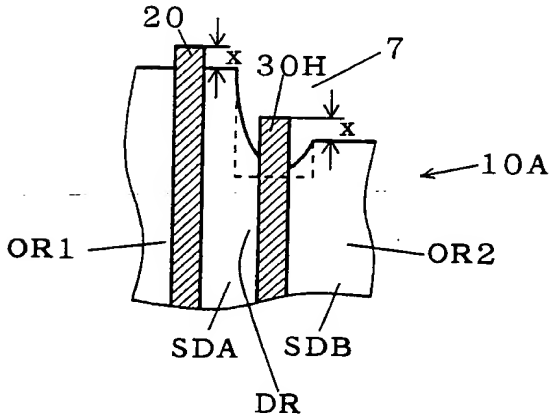

FIG. 26

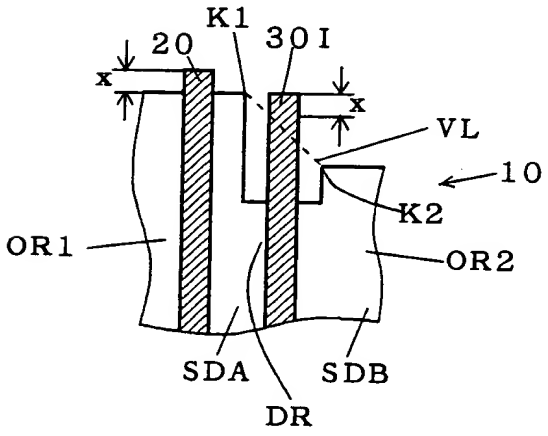

FIG. 27

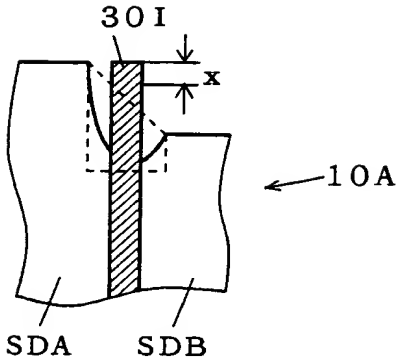

FIG. 28

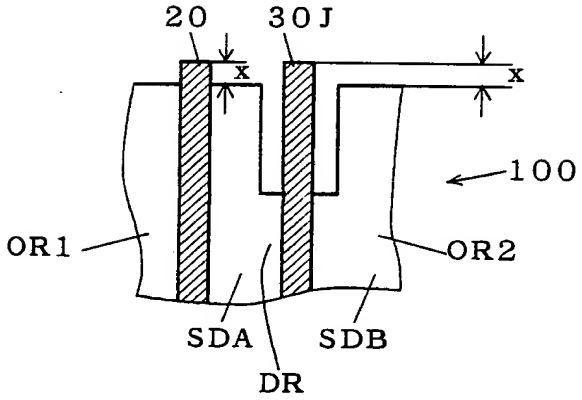

FIG. 29 (BACKGROUND ART)